superposition.

23. (New) A method according to claim 20 further comprising converting at least one of the image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

A7

IN THE ABSTRACT

Please replace the Abstract at page 22, lines 1-9 as follows:[3]

ABSTRACT

The overlay image processing device comprises: an image selector for selecting from among image signals one reference image signal and superimposing image signals; a resolution converter for converting resolutions of the selected image signals including the reference image signal and the superimposing image signals into respective desired resolutions; and an image synthesizer for superimposing the converted superimposing image signals on the converted reference signal.

A8

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-15 are pending in the present application. Claims 1, 2, 4-6, and 9-15 are amended, and new Claims 16-23 are added by the present amendment.

[3] A marked-up copy of the changes made to the Abstract is attached.

In the outstanding Office Action, the specification and Claim 5 were objected to. Claims 1, 6, and 11 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-15 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,157,415 to Glen.

Applicants thank the Examiner for the courtesy of an interview extended to Applicants' representatives on April 23, 2003. During the interview, the patentability of the claims over the applied art was discussed. No agreement was reached pending updated search and review after a response is filed.

Regarding the objection to the specification and Claim 5, the specification and Claim 5 have been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copies. In addition, Claims 1, 2, 4-6, and 9-15, the specification, and the abstract are amended to correct minor grammatical informalities and to conform to standard patent practice. It is believed no new matter has been added. Accordingly, it is respectfully requested that objection be withdrawn.

Further, regarding the rejection of Claims 1, 6, and 11 under 35 U.S.C. § 112, second paragraph, Claims 1, 6, and 11 are amended in light of the comments noted in the outstanding Office Action and to recite "an image selector configured to select from among the plurality of digitally decoded image signals one reference image signal and (n-1) number of superimposing image signals." It is believed no new matter has been added. Accordingly, it is respectfully requested that rejection be withdrawn.

Claims 1-15 were rejected under 35 U.S.C. § 102(e) as anticipated by Glen. That rejection is respectfully traversed.

Amended Claim 1 is directed to an overlay image processing device including "a plurality of digital decoders configured to digitally decode a plurality of image signals" and "an image selector configured to receive outputs from each of the plurality of digital decoders and configured to select from among the plurality of digitally decoded image signals one

reference image signal and (n-1) number of superimposing image signals," support for which is found in the originally filed specification at least in Figure 2 and at page 5, line 21, to page 6, line 24. In addition, the overlay image processing device includes:

> a plurality of resolution converters configured to receive respective outputs of the image selector such that any resolution converter can receive any output of the image selector, the plurality of resolution converters further configured to convert resolutions of the *n* number of selected image signals including the reference image signal and the (*n*-1) number of superimposing image signals into respective desired resolutions...

Support for the features of Claim 1 is found in the originally filed specification at least in Figure 2 and at page 1, line 23, to page 2, line 9. Independent Claims 6 and 11 are amended to include similar features.

In a non-limiting example, Figure 3 shows that a digital decoder 110 converts the analog computer signal VPC(A) into the digital computer signal VPC(D). The second and third digital decoders 112, 114 convert the analog television signals VS1(A), VS2(A) into digital television signals VS1(D), VS2(D) (see the specification at page 5, lines 7-20).

Further, Figure 2 shows the selector 116 selects two image signals from among the three original digitized image signals VPC(D), VS1(D), and CS2(D), according to a user's instruction. One of the two selected original image signals is designated as a reference original image signal SD10, or background image signal, and the other as a superimposing original image signal SD20. One of the two selected original image signals is designated as a reference original image signal SD10, or background image signal, and the other as a superimposing original image signal SD20 (see the specification at page 6, lines 18-24). The first resolution converter 118 converts the resolution of the reference original image signal SD10 to produce a reference image signal SD1, and the second resolution converter 120 converts the resolution of the superimposing original image signal SD20 to produce a superimposing image signal SD2 (see the specification at page 6, lines 25-30).

As an advantage, flexibility is facilitated because any resolution converter can receive as an input the digitally decoded signal from any of the digital decoders (see the specification at page 11, line 23, to page 12, line 2).

In contrast, Glen only discusses a system in which "the multiplexor 100 ... selects one of the output signals. The selected input signal is passed to the programmable color base converting module 102" (see Glen at column 8, lines 4-15). Also, Figures 2 and 6A-6C of Glen show that various signals such as "RGB in," "TV in," and "HDTV in" of different "color bases" are input directly to a "mux 100," without digital decoders first digitally decoding the input signals. That arrangement differs from the system of the pending claims, in which an image selector selects "from among the plurality of digitally decoded image signals" that are digitally decoded by a plurality of digital decoders.

Moreover, Figures 6A-6C of Glen show a system in which only certain subsets of image inputs can be fed to various "blend modules" (76, 78, 80). Because the "blend modules" according to Glen are specialized to blend input signals of a particular format, e.g. an "RGB blend module 76" or a "TV blend module 80," those "blend modules" cannot receive as an input ***any*** of the signals output from a selector, as in the pending claims.

Accordingly, it is respectfully submitted that independent Claims 1, 6, 11, and each of the claims depending therefrom are allowable.

In addition, new Claims 16-23 are added to set forth the invention in a varying scope. New Claim 16 is similar to Claim 1, and further recites:

> an image synthesizer configured to superimpose the (n-1) number of converted superimposing image signals on the converted reference signal, the image synthesizer including first and second overlay processors connected in series, the first overlay processor configured to receive an output from a subset of the plurality of resolution converters, and the second overlay processor configured to directly receive an output from the first overlay processor and another of the plurality of resolution converters.

New Claim 20 is a method claim including similar features, support for which is found in the originally filed specification at least in Figure 11 and at page 12, line 24, to page 13, line 24. New Claims 17-19 and 21-23, which depend on new Claims 16 and 20, respectively, are similar to Claims 2-4 and 12-14. It is believed that no new matter has been added.

As discussed, the features of Claims 1 and 11 are believed to patentably distinguish over Glen. In addition, the features of new Claims 16 and 20 further distinguish over Glen for at least the following reasons.

In a non-limiting example, Figure 11 shows two OVL processors 132, 130 implementing two-stage image overlay. In the overlay image processing device 10B, the reference image signal and superimposing image signals can be selected arbitrarily by the selector 116 from among three input image signals, whereby three images can be overlaid in an arbitrary order of preference. As an advantage, the overlay processing device 10B can arbitrarily select a single reference image signal from among three image signals, and arbitrarily select the remaining two image signals as superimposing image signals. The two selected superimposing image signals can then be superimposed in an arbitrary order of preference over the selected reference image signal to generate an overlay image signal (see the specification at page 13, lines 6-10, and page 13, line 25, to page 14, line 6).

In addition, Figure 11 shows that the first overlay image signal OD1, which is produced as an output of a first overlay processor 132, is supplied directly to a second overlay processor 130. Thus the system of the pending claims advantageously does not require a resolution converter between the first and second overlay processors.

In contrast, Figures 5A-5C of Glen only show an arrangement in which a "color base converter 84" is required between a first "TV blend module 80" and a second "RGB blend module 76." Glen does not teach or suggest an overlay image processing device in which a

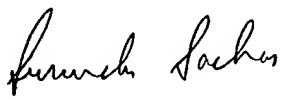
second overlay processor directly receives an output from a first overlay processor, as in new Claims 16 and 20.

Accordingly, it is respectfully submitted that new Claims 16 and 20, and each of the claims depending therefrom, even further patentably distinguish over Glen.

Consequently, in light of the above discussion and in view of the present amendment, this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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IN THE SPECIFICATION

Please replace the paragraph at page 1, lines 8-16, as follows:

Certain projectors and other such image display devices are capable of simultaneously displaying image signals from a number of different types of image providing devices. Such devices are capable of simultaneously displaying, for example, [a] images played back by a video tape recorder or images taken with a video camera, superimposed over a graphic image generated by a personal computer. The superimposition of other images ("superimposed images" hereinafter) over a single image ("reference image" hereinafter) is termed "overlay." Hereinafter, images displayed in overlay mode are termed "overlay images."

Please replace the paragraph at page 2, lines 8-19, as follows:

In a preferred embodiment, the image synthesizer has the *n* number of 2-input image synthesizers, where each 2-input image synthesizer is configured to [receives] receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal. The *n* number of 2-input image synthesizers are connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of an i^{th} stage, where *i* is between 2 and *n*, inclusive, uses an output of the 2-input image synthesizer of an $(i\text{-}1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image

signal.

Please replace the paragraph at page 5, lines 7-11, as follows:

In the preceding manner, the first digital decoder 110 converts the analog computer [signals] signal VPC(A) into the digital computer [signals] signal VPC(D). The digital computer signal VPC(D) contains the digital RGB signal DRGBpc, horizontal sync signal HDpc, vertical sync signal VDpc, and clock signal SCLKpc.

IN THE CLAIMS

1. (Amended) An overlay image processing device for generating an overlay image signal composed of an *n* number of superimposed image signals, *n* being an integer greater than [1] 2, the overlay image processing device comprising:

a plurality of digital decoders configured to digitally decode a plurality of image signals;

an image selector configured to receive outputs from each of the plurality of digital decoders and configured to select from among [an *m* number] the plurality of digitally decoded image signals one reference image signal and (*n*-1) number of superimposing image signals[, *m* being an integer greater than 2];

a plurality of resolution [converter] converters configured to receive respective outputs of the image selector such that any resolution converter can receive any output of the image selector, the plurality of resolution converters further configured to convert resolutions of the *n* number of selected image signals including the reference image signal and the (*n*-1) number of superimposing image signals into respective desired resolutions; and

an image synthesizer configured to superimpose the (n-1) number of converted superimposing image signals on the converted reference signal.

2. (Amended) An overlay image processing device according to claim 1 wherein at least one of the [m number] plurality of image signals is a display signal output from a personal computer.

4. (Amended) An overlay image processing device according to claim 1 further comprising a scan converter [that, in the event that at least one of the n number of image signals selected by the image selector is an interlaced image signal, coverts the] configured to convert at least one of the interlaced image [signal] signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

5. (Amended) An overlay image processing device according to claim 1 wherein the image synthesizer has the n number of 2-input image synthesizers, each 2-input image synthesizer being configured to [receives] receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal;

the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of an i^{th} stage, where i is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of an $(i\text{-}1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image signal.

6. (Amended) An overlay image display device for displaying an overlay image composed of an *n* number of superimposed images, *n* being an integer greater than [1] 2, the overlay image display device comprising:

an overlay image processing device for generating an overlay image signal composed of the *n* number of superimposed image signals; and

an image display device for displaying an image represented by the overlay image signal;

wherein the overlay image processing device includes:

a plurality of digital decoders configured to digitally decode a plurality of image signals;

an image selector configured to receive outputs from each of the plurality of digital decoders and configured to select from among [an *m* number] the plurality of digitally decoded image signals one reference image signal and (*n*-1) number of superimposing image signals[, *m* being an integer greater than 2];

a plurality of resolution [converter] converters configured to receive respective outputs of the image selector such that any resolution converter can receive any output of the image selector, the plurality of resolution converters further configured to convert resolutions of the *n* number of selected image signals including the reference image signal and the (*n*-1) number of superimposing image signals into respective desired resolutions; and

an image synthesizer configured to superimpose the (*n*-1) number of converted superimposing image signals on the converted reference signal.

9. (Amended) An overlay image display device according to claim 6 further comprising a scan converter [that, in the event that at least one of the *n* number of image

signals selected by the image selector is an interlaced image signal, coverts the] configured to convert at least one [interlaced] of the image [signal] signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

10. (Amended) An overlay image display device according to claim 6 wherein the image synthesizer has the *n* number of 2-input image synthesizers, each 2-input image synthesizer being configured to [receives] receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal;

the *n* number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of an i^{th} stage, where *i* is between 2 and *n*, inclusive, uses an output of the 2-input image synthesizer of an $(i\text{-}1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image signal.

11. (Amended) A method of generating an overlay image signal composed of an *n* number of superimposed image signals, *n* being an integer greater than [1] 2, the method comprising the steps of:

(a) digitally decoding a plurality of image signals;

(b) receiving outputs from each of a plurality of digital decoders;

[(a)] (c) selecting from among [an *m* number] the plurality of digitally decoded image signals one reference image signal and (*n*-1) number of superimposing image signals[, *m* being an integer greater than 2];

[(b)] (d) converting resolutions of the *n* number of selected image signals including the reference image signal and the (*n*-1) number of superimposing image signals into respective desired resolutions by receiving respective outputs of the step (c) such that any resolution conversion can receive any output of the step (c); and

[(c)] (e) superimposing the (*n*-1) number of converted superimposing image signals on the converted reference signal.

12. (Amended) A method according to claim 11 wherein at least one of the [*m* number] plurality of image signals is a display signal output from a personal computer.

13. (Amended) A method according to claim 11 wherein the step [(a)] (c) includes [the step of] selecting the reference image signal and the (*n*-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the *n* number of image signals; and

the step [(c)] (e) includes [the step of] superimposing the (*n*-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

14. (Amended) A method according to claim 11 further comprising [a step of, in the event that at least one of the *n* number of image signals selected by the image selector is an interlaced image signal,] converting [the] at least one [interlaced] of the image [signal] signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

15. (Amended) A method according to claim 11 wherein the step [(c)] (e) includes the *n* number of 2-input image synthesizing steps, each 2-input image synthesizing step including receiving upper-side and lower-side image signals and superimposing [the] an upper-side image signal on [the] a lower-side image signal;

the *n* number of 2-input image synthesizing steps being performed in series in multistage fashion such that the 2-input image synthesizing step of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizing step of an i^{th} stage, where *i* is between 2 and *n*, inclusive, uses an output of the 2-input image synthesizing step of an $(i\text{-}1)^{th}$ stage as the lower-side image signal and an i^{th} superimposing image signal as the upper-side image signal.

16-23. (New)

IN THE ABSTRACT

ABSTRACT [OF THE DISCLOSURE]

The overlay image processing device comprises: an image selector for selecting from among [an *m* number of] image signals one reference image signal and [(*n*-1) number of] superimposing image signals[, where *m* is an integer greater than 2]; a resolution converter for converting resolutions of the [*n* number of] selected image signals including the reference image signal and the [(*n*-1) number of] superimposing image signals into respective desired resolutions; and an image synthesizer for superimposing the [(*n*-1) number of] converted superimposing image signals on the converted reference signal.